What is Claimed is:

1. A method for conversion of signals, comprising:

receiving a first plurality of bits from a first signal;

performing a look-up in a table with a first subset of bits in the first plurality of bits to generate a result;

adding the result to a sum;

performing another look-up in the table with the next subset of bits in the first plurality of bits and adding the result to the sum until a look-up with a last subset of bits in the first plurality of bits is performed and the result added to sum;

providing the sum as a first multiple bit value of a second signal; and

receiving a second plurality of bits from the first signal and converting to a second multiple bit value of the second signal using the steps described above until all bits in the first signal have been converted.

2. The method of Claim 1, wherein the first signal is a direct stream digital (DSD) signal.

3. The method of Claim 1, wherein the second signal is a pulse code modulated (PCM) signal.

4. The method of Claim 1, wherein each plurality of bits has the same number of bits and each subset of bits in the plurality of bits has the same number of bits.

5. The method of Claim 4, wherein the table is a two dimensional array containing a plurality of elements, the size of the first dimension equal the number of bits in the plurality of bits divided by the number of bits in the subset of the plurality of bits, the size of the second dimension equal to $2^{(\text{number of bits in subset})}$.

6. The method of Claim 5, wherein each element contains one multiple bit result, wherein performing the look-up in the table comprises accessing the element in the array that corresponds to the number of the subset in the plurality of bits and the value of the subset of bits.

7. A method for conversion of direct stream digital (DSD) signals to pulse code modulated (PCM) signals, comprising:

receiving a first plurality of bits from the DSD signal;

performing a look-up in a table with a first word in the first plurality of bits to generate a result;

adding the result to a sum;

performing another look-up in the table with the next word in the first plurality of bits and adding the result to the sum until a look-up with a last word in the first plurality of bits is performed and the result added to sum;

providing the sum as a first multiple bit value of a PCM signal; and

receiving a second plurality of bits from the DSD signal and converting to a second multiple bit value of the PCM signal using the steps described above until all bits in the DSD signal have been converted.

8. The method of Claim 7, wherein each plurality of bits has the same number of bits and each word in the plurality of bits has the same number of bits.

9. The method of Claim 8, wherein the table is a two dimensional array containing a plurality of elements, the size of the first dimension equal the number of bits in the plurality of bits divided by the number of bits in the word, the size of the second dimension equal to $2^{(\text{number of bits in word})}$.

10. The method of Claim 9, wherein each element contains one multiple bit result, wherein performing the look-up in the table comprises accessing the element in the array that corresponds to the number of the word in the plurality of bits and the value of the word.

11. An apparatus for conversion of signals, comprising:

a first-in-first-out (FIFO) buffer that contains a plurality of bits from a first signal, wherein the plurality of bits is further divided into a plurality of subset of bits of the same size;

a look-up table coupled to the FIFO buffer, wherein the look-up table generates a result for each of the plurality of subset of bits; and

an accumulator coupled to the look-up table, the accumulator holding the results added together, wherein after adding the result for the last subset of bits in the plurality of bits, the accumulator generates at an output a multiple bit second signal.

12. The apparatus of Claim 11, further comprising an address generator connected to the FIFO buffer and look-up table, said address generator providing to the look-up table the address of a section in the look-up table corresponding to each of the plurality of subset of bits, each of said sections including a plurality of results for each subset of bits, wherein the value of the subset of bits selects one of the plurality of results.

13. The apparatus of Claim 12, wherein the address of each section in the look-up table corresponding to each of the plurality of subset of bits is sequential.

14. The apparatus of Claim 11, wherein the first signal is a direct stream digital (DSD) signal.

15. The apparatus of Claim 11, wherein the second signal is a pulse code modulated (PCM) signal.

16. The apparatus of Claim 11, wherein the look-up table is contained in a memory located on a digital signal processor (DSP).

17. The apparatus of Claim 11, wherein the look-up table is contained in an external memory coupled to a digital signal processor (DSP).

18. An apparatus for conversion of direct stream digital (DSD) signals to pulse code modulated (PCM) signals, comprising:

a first-in-first-out (FIFO) buffer that contains a plurality of bits from the DSD signal, wherein the plurality of bits is further divided into a plurality of words of the same size;

a look-up table coupled to the FIFO buffer, wherein the look-up table generates a result for each word; and

an accumulator coupled to the look-up table, the accumulator holding the results added together, wherein after adding the result for the last word in the plurality of bits, the accumulator generates at an output a multiple bit PCM signal.

19. The apparatus of Claim 18, further comprising an address generator connected to the FIFO buffer and look-up table, said address generator providing to the look-up table the address of a section in the look-up table corresponding to each of the plurality of words, each of said sections including a plurality of results for each word, wherein the value of the word selects one of the plurality of results.

20. The apparatus of Claim 18, wherein the look-up table is contained in a memory located on a digital signal processor (DSP).

21. The apparatus of Claim 18, wherein the look-up table is contained in an external memory coupled to a digital signal processor (DSP).

22. An apparatus for conversion of signals, comprising:

means for receiving a first plurality of bits from a first signal;

means for performing a look-up in a table with a first subset of bits in the first plurality of bits to generate a result;

means for adding the result to a sum;

means for performing another look-up in the table with the next subset of bits in the first plurality of bits and adding the result to the sum until a look-up with a last subset of bits in the first plurality of bits is performed and the result added to sum;

means for providing the sum as a first multiple bit value of a second signal; and

means for receiving a second plurality of bits from the first signal and converting to a second multiple bit value of the second signal using the steps described above until all bits in the first signal have been converted.